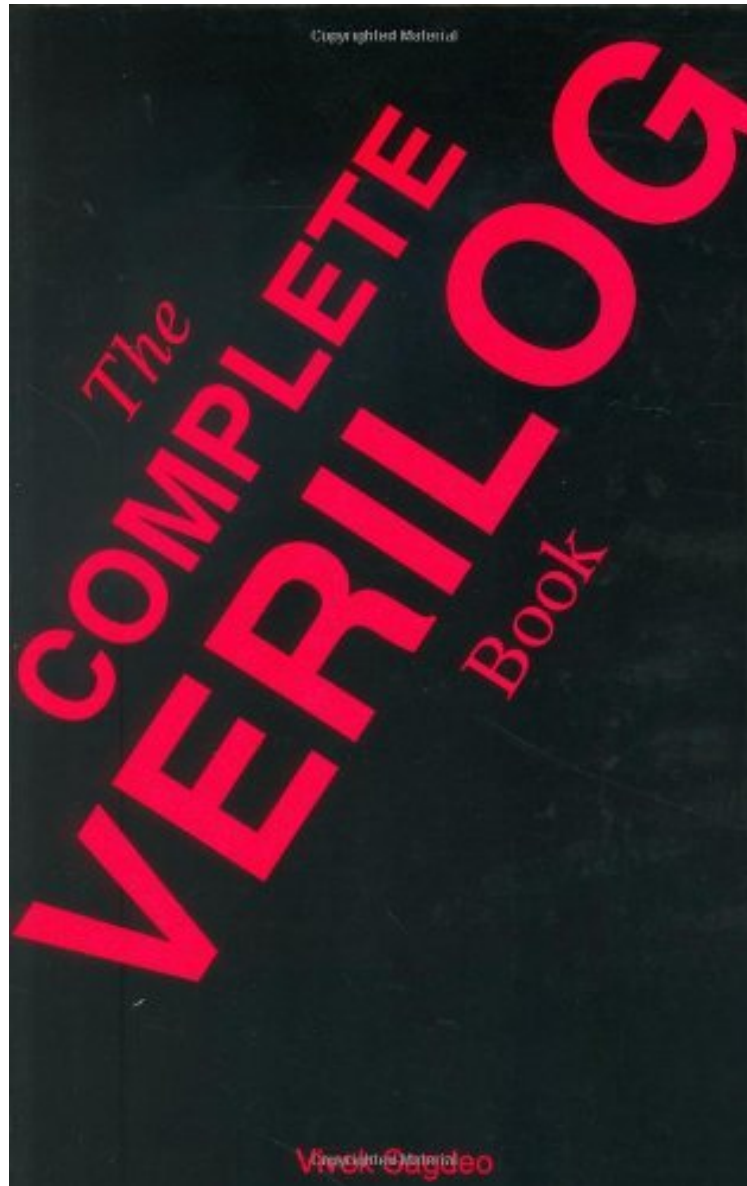


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The Complete Verilog Book

Von Vivek Sagdeo

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Von Vivek Sagdeo : The Complete Verilog Book before purchasing it in order to gage whether or not it would be worth my time, and all praised The Complete Verilog Book:

KundenrezensionenHilfreichste Kundenrezensionen0 von 0 Kunden fanden die folgende Rezension hilfreich. Good reference mediocre for learning.Von Ein KundeThe book has plenty of code samples, however, many of them have mistakes, making it difficult and sometimes frustrating to study the code. The explanations are not well written when

compared to other books (Thomas and Moorby's), however there is some information that cannot be found in other books. An excellent book except for the price and mistakes on nearly every page. If you are already experienced in Verilog, this may be an excellent reference, however, if you are just learning, Thomas Moorby's "The Verilog Hardware Description Language" is an excellent and highly recommended book. 0 von 0 Kunden fanden die folgende Rezension hilfreich. a great book with almost everything for designers to referenVon Ein KundeThis book is really a worthwhile book to read and study for advanced topics of designs based on Verilog and Synopsys synthesis tools. The feature-rich topics and details of how the constructs of the designs are made are quite clear and well-written for people involved. The only thing I'm concerned is the price seems to be way way too high to general reader, as it's \$135 before tax. Hopefully the price can drop at least 40% less so that everybody can buy it. regards, JKL, San Jose, Calif.

KurzbeschreibungThe Verilog hardware description language (HDL) provides the ability to describe digital and analog systems. This ability spans the range from descriptions that express conceptual and architectural design to detailed descriptions of implementations in gates and transistors. Verilog was developed originally at Gateway Design Automation Corporation during the mid-eighties. Tools to verify designs expressed in Verilog were implemented at the same time and marketed. Now Verilog is an open standard of IEEE with the number 1364. Verilog HDL is now used universally for digital designs in ASIC, FPGA, microprocessor, DSP and many other kinds of design-centers and is supported by most of the EDA companies. The research and education that is conducted in many universities is also using Verilog. This book introduces the Verilog hardware description language and describes it in a comprehensive manner. Verilog HDL was originally developed and specified with the intent of use with a simulator. Semantics of the language had not been fully described until now. In this book, each feature of the language is described using semantic introduction, syntax and examples. Chapter 4 leads to the full semantics of the language by providing definitions of terms, and explaining data structures and algorithms. The book is written with the approach that Verilog is not only a simulation or synthesis language, or a formal method of describing design, but a complete language addressing all of these aspects. This book covers many aspects of Verilog HDL that are essential parts of any design process.

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SynopsisThe Verilog hardware description language provides the ability to describe digital and analogue systems for design concepts and implementation. It was developed originally at Gateway Design and implemented there. Now it is an open standard of IEEE and Open Verilog International and is supported by many tools and processes. This volume introduces the language and describes it in a comprehensive manner. In the book, each feature of the language is described using semantic introduction, syntax and examples. A chapter on semantics explains the basic concepts and algorithms that form the basis of every evaluation and every sequence of evaluations that ultimately provides the meaning or full semantics of the language. The book takes the approach that Verilog is not only a simulation language or a synthesis language or a formal method of describing design, but is a totality of all these and covers many aspects not covered before, but which are essential parts of any design process using Verilog. The text explains the data types in Verilog HDL, as the object-oriented world knows that the language-constructs and data types are equally important parts of a language. It explains the three views, behavioural, RTL and structural, and then describes features in each of these views. The volume aims to keep the reader abreast of developments in the Verilog world such as Verilog-A, cycle simulation, SD, and DCL, and uses IEEE 1364 syntax.